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Porous $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ thin film cathodes for large area micro solid oxide fuel cell power generators

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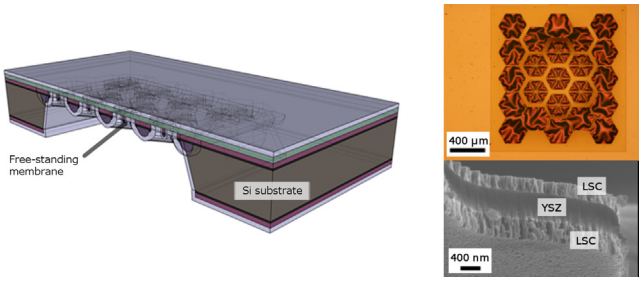
HIGHLIGHTS

- Porous LSC thin film cathodes were implemented in real micro SOFC configuration.
- LSC/YSZ/LSC symmetrical free-standing membranes fully integrated on silicon.
- Thermo-mechanical stability of the all-ceramic membrane is shown up to 700 °C.
- LSC/YSZ interfaces show area specific resistance below 0.3 Ω cm^2 at $T = 700$ °C.
- LSC presented as a good alternative to metallic electrodes for reliable micro SOFC.

GRAPHICAL ABSTRACT



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ABSTRACT

Porous $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ thin films were fabricated by pulsed laser deposition for being used as a cathode for micro solid oxide fuel cell applications as MEMS power generators. Symmetrical $La_{0.6}Sr_{0.4}CoO_{3-\delta}$/yttria-stabilized zirconia/$La_{0.6}Sr_{0.4}CoO_{3-\delta}$ free-standing membranes were fabricated using silicon as a substrate. A novel large-area membrane design based on grids of doped-silicon slabs was used. Thermo-mechanical stability of the tri-layer membranes was ensured in the intermediate range of temperatures up to 700 °C. In-plane conductivity of *ca.* 300 S cm^{-1} was measured for the cathode within the whole range of application temperatures. Finally, area specific resistance values below 0.3 Ω cm^2 were measured for the cathode/electrolyte bi-layer at 700 °C in the exact final micro solid oxide fuel cell device configuration, thus presenting $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ as a good alternative for fabricating reliable micro solid oxide fuel cells for intermediate temperature applications.

1. Introduction

Miniaturization of solid oxide fuel cells (SOFCs) has been recently proposed as a promising alternative for powering portable devices [1,2]. The micro SOFC (μSOFC) concept is based on the development of ultra-thin electrolytes supported on low thermal

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mass structures [3–9]. This combination keeps the main benefits of SOFC technology, i.e. high specific energy per unit mass and volume, efficiency and fuel flexibility, while overcoming its major drawbacks, namely, high operating temperatures and long and high-power-consumption start-up processes. Different designs have been reported in the literature, most of them based on free-standing electrolyte membranes supported on silicon-based substrates. The integration of SOFCs in micro electromechanical systems (MEMS) technology becomes crucial to achieve the desired miniaturization while ensuring high reproducibility, cheap mass production and electronics compatibility.

In this sense, big efforts have been devoted to the development of optimized membrane designs, i.e. maximizing the membrane active area while ensuring structural and thermomechanical stability, in order to enlarge the total power achievable per single device. Opposed to original simple squared membrane designs with a limited maximum size [3], recent works focus on the fabrication of membranes with enlarged areas reaching several mm^2. First Rey-Mermet et al. [10] and lately Ramanathan et al. [4] used dense Ni grids as robust support for fabricating membranes with a maximum area of 25 mm^2. This way, a maximum power output multiplied by a factor of $\times 30$ has been achieved. A second alternative for increasing the active area was reported by Su et al. [7]. It consists on the fabrication of corrugated membranes with surface utilization increased by 30%–64%. This allows almost doubling the maximum power of the μSOFC.

Great performances have been reported by μSOFCs based on thin film free-standing YSZ electrolytic membranes, both using the basic squared designs and the large-area ones. YSZ membranes present thermo-mechanical stability through the whole intermediate temperature range (up to 700 °C), and reach the target value usually established for the Area Specific Resistance (ASR = 0.15 Ω cm^2, [11]) at temperatures as low as 400 °C [6,12]. However, despite the good performance achieved by the thin electrolytes themselves and the promising works reported on μSOFC devices (a maximum power density of 1037 mW cm^{-2} was reported by Kerman et al. [13]), the quick degradation shown by the typically implemented metallic electrodes [3,14] at operating temperatures still hinders the way to the commercialization of μSOFC devices [15–17]. A difficult balance between two opposite phenomena is required for the development of reliable metallic-based thin film electrodes, namely: (i) the promotion of thin film dewetting with temperature, in order to form a porous film and enlarge the triple phase boundary (TPB) length without losing the connectivity; (ii) the limitation of the dewetting process that makes the thin films unstable at operating temperatures. This last phenomenon leads to the agglomeration of the metal during operation yielding the formation of isolated metallic islands, with the loss of in-plane percolation and/or dramatic reduction of active area. Fast degradation of metallic thin films implemented on μSOFC configurations have been already reported by Ramanathan et al. [4,13,18].

As a consequence of this, the implementation of more reliable and stable thin film ceramic-based electrodes into μSOFC systems seems to be the next natural goal for the μSOFC community. Indeed, some attempts have been already reported on the development of pure oxide-based electrodes for fabricating fully-ceramic μSOFC, based on state-of-the-art materials on bulk SOFC systems working as cathodes [19–27] or anodes [28]. However, only few results have been reported on μSOFC performance using ceramic electrodes [29–32].

Lanthanum strontium cobaltite (LSC) is one of the most extended and studied cathode materials for SOFCs, especially when working in the intermediate range of temperatures. Reactivity issues between LSC and yttria-stabilized zirconia (propensity to form insulating $La_2Zr_2O_7$ or $SrZrO_3$ phases in the cathode/YSZ interface [33–35]) together with the large mismatch in the thermal expansion coefficient of LSC vs. YSZ ($TEC_{LSC} = 23$ ppm K^{-1}; $TEC_{YSZ} = 11$ ppm K^{-1} [36–38]) limit its applicability at high operating temperatures or in devices involving high T fabrication steps ($T > 700$ °C). In this sense, alternative electrolytes or barrier diffusion layers are sometimes introduced between the electrolyte and the cathode for reducing these effects but still degradation by detachment is present [39–41]. The implementation of the LSC layer in porous thin film form has been recently proposed as a good solution for this particular problem showing very promising results in the intermediate range of temperatures ($T < 700$ °C) [21–23,42]. It is important to notice here that either increasing the density of LSC thin films (internal lattice strain fields involved, [43–46]) or lowering the pO_2 [47] can induce Sr segregation and mid-term quick degradation.

In this work, porous thin films of $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ were fabricated and tested as cathodes in free-standing membranes of dense yttria-stabilized zirconia working as an electrolyte. Porous electrode and dense electrolyte were deposited by Pulsed Laser Deposition (PLD) by using different deposition conditions. The all-PLD-deposited symmetrical cells (LSC/YSZ/LSC) were supported on a novel large-area free-standing membrane design [48–50]. This new membrane design is based on the use of a grid of doped silicon slabs as support. Opposed to the previous strategies (based on metallic grids), the here-presented strategy is fully based on silicon, thus compatible with CMOS and MEMS technology.

In order to evaluate the suitability of LSC for thin film μSOFC cathodes, in-plane conductivity measurements were performed on simple films, to ensure good current collection, and a complete electrochemical characterization of the symmetrical free-standing membrane (half-cell measurements) was carried out, to evaluate the optimum operation temperature range of the LSC/YSZ (cathode/electrolyte) bilayer.

2. Experimental

2.1. Pulsed Laser Deposition and characterization of porous LSC films on bulk substrates

Yttria-stabilized zirconia (8 mol% Y_2O_3–ZrO_2 – YSZ) and $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ (LSC) pellets were fabricated by conventional sintering for being used as targets for PLD. Starting from a commercial powder of YSZ (Tosoh) and LSC powder supplied by EMPA (Switzerland), green pellets were obtained by compaction in a uniaxial die press. Sintered discs were obtained after a thermal treatment at 1450 °C for 7 h in air achieving relative densities over 95%.

Dense YSZ thin films of 200–500 nm thick were deposited by PLD over $Si_3N_4/SiO_2/Si$ substrates by laser ablation of the previously fabricated target. Details on the substrate fabrication and PLD deposition conditions to obtain dense and homogeneous YSZ films are described with greater detail elsewhere [6]. Porous LSC films were deposited by PLD over the YSZ films. In order to achieve the desired porosity, a higher base pressure was employed, i.e. $1.0 \cdot 10^{-1}$ mbar instead of $2.5 \cdot 10^{-2}$ mbar. Deposition temperature was also lowered from 600 °C (dense YSZ) to 100 °C (porous LSC). The deposition time for obtaining 350 nm thick films of LSC was 25 min, using a pulse rate of 10 Hz and laser energy of 1 J cm^{-2}. A PLD5000 equipment from PVD was used for the functional layers deposition at a wafer level, allowing the integration of the technique onto the silicon substrate fabrication flow. The so-prepared bi-layer samples were used in this work for the study of the electrode microstructure and in-plane electrical conductivity.

Scanning electron microscopy (SEM, Zeiss Auriga) was used for the study of the microstructure of LSC deposited films before and after thermal treatments up to the maximum working temperature ($T = 700$ °C). The identification of the phase on the films and its

evolution with temperature was made by in situ X-ray diffraction (XRD, Brucker-D8 Advance). A temperature-controlled stage was employed for the acquisition of diffraction patterns at different temperatures, from room temperature to 700 °C in steps of 50 °C.

In-plane electrical characterization of the as-deposited porous LSC films was carried out by using the Van der Pauw method [51]. Four gold electrodes were painted on top of the LSC films (close to the corner edges) for their use as electrical contacts. Measurements at different temperatures, ranging from room temperature to 700 °C, were carried out on a Probostat cell placed inside a furnace by means of a Keithley 2400 sourcemeter, using slow heating and cooling ramps (1 °C min^{-1}). A constant flux of synthetic air was forced in order to provide with the desired oxidizing atmosphere. A thermocouple was located besides the sample for temperature control.

2.2. Fabrication and characterization of large-area self-supported membranes of LSC/YSZ/LSC

LSC/YSZ/LSC free-standing membranes were fabricated for testing LSC as a cathode on a real μSOFC configuration. The technological flow for the fabrication of the self-supported low-thermal mass membranes is described in Fig. 1a and references [48–50]. In order to make large area thermo-mechanically stable membranes, a grid of doped-silicon slabs was defined in the earlier stages of micro fabrication (photolithographic step followed by a doping process [52], step *A* in Fig. 1a). A SiO_2/Si_3N_4 dielectric bi-layer is then deposited on both sides of the substrate serving as isolation and substrate for the functional layer deposition (step *B*). By a second photolithographic step from the back side (step *C*) the Si_3N_4 layer is selectively removed (using Reactive Ion Etching, RIE), thus defining the zone of the silicon substrate to be etched for obtaining the membranes. SiO_2 and Si are wet etched (HF and KOH, respectively) from the back side using the Si_3N_4 layer as mask (step *D*). After these etching processes, Si_3N_4 free-standing membranes supported on hexagonal doped silicon slabs grids were obtained on the top side (see Fig. 1b–c). Doped silicon zones were not etched due to their high selectivity to Si anisotropic etchants (KOH), thus the silicon slabs grids were obtained [52]. The obtained membranes ranged from 1.8 × 1.8 mm^2 to 3.5 × 3.5 mm^2 and were used as substrate for the electrolyte deposition. These membranes present tensile strain and are used as sacrificial layers for the PLD deposition of the functional dense 500 nm YSZ electrolytes (same deposition conditions than in previous section). By removing the silicon nitride layer, using selective reactive ion etching (RIE), YSZ free-standing membranes were released allowing a double side deposition of porous LSC of 350 nm thick (same deposition conditions than in previous section) to define the symmetrical LSC/YSZ/LSC cells. Finally, patterned 150 nm thick Pt films were implemented on both sides of the membrane to serve as current collectors. The mentioned pattern was defined by nanosphere lithography as detailed elsewhere [49], maintaining a substantial porosity after high temperature characterization. Comparison between top view SEM images on Fig. 2 show the microstructure evolution of the Pt

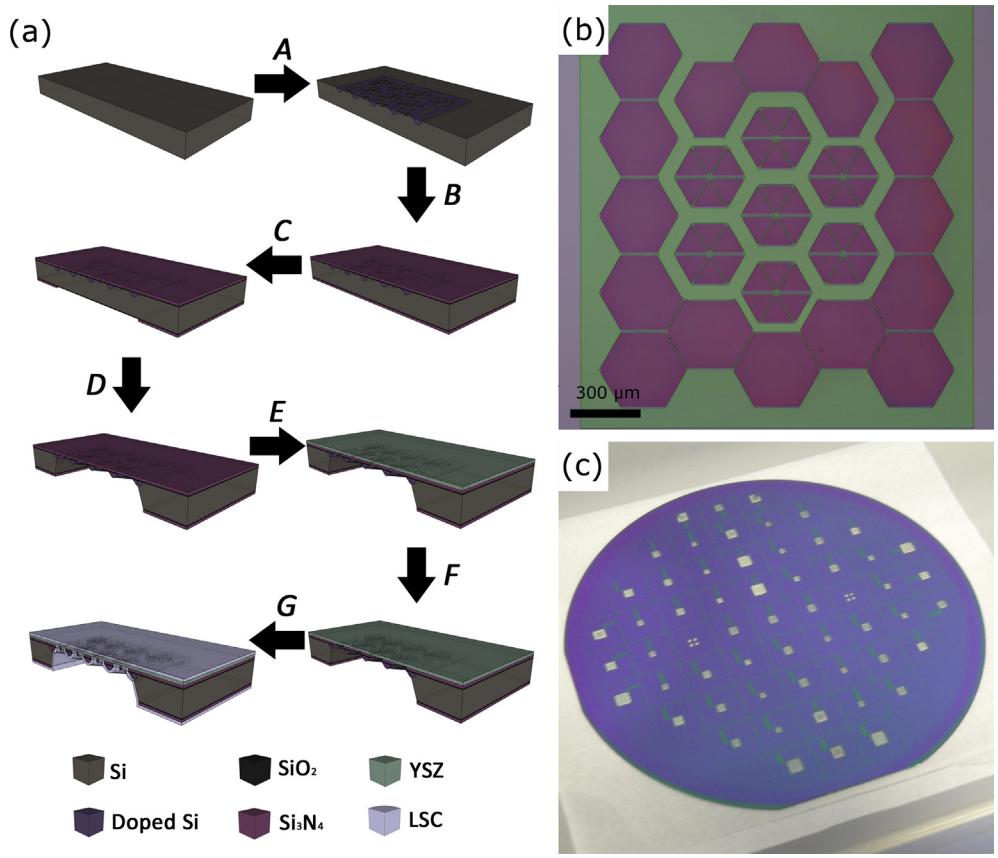

Fig. 1. (a) Main steps of the fabrication process flow of large-area LSC/YSZ/LSC self-supported membranes. First, a photolithographic step defines the doped silicon slabs where the ceramic films will stand (A); then, a SiO_2/Si_3N_4 dielectric bi-layer is deposited on both sides of the substrate (B); a second photolithographic step from the back side (C) selectively eliminates the Si_3N_4 layer defining the zone to be etched for obtaining the membranes on the opposite side; SiO_2 and Si are wet etched from the back side using the Si_3N_4 layer as mask (D), obtaining large-area Si_3N_4 membranes on the top side; dense YSZ layers are deposited over the Si_3N_4 by PLD (E); a RIE step eliminates the remaining Si_3N_4 layer releasing free-standing YSZ membranes (F); finally, porous LSC layers are deposited on both sides of the substrate by PLD, forming free-standing LSC/YSZ/LSC membranes (G). (b) Detail of a large-area Si_3N_4 membrane, before YSZ deposition by PLD (step (D)). (c) Processed wafer after step (D), used as substrate for large-area PLD deposition.

mesh after measurements performed at high $T = 700\ ^{\circ}C$, revealing a microstructural change during the measurement but in any case losing the porosity and connectivity on the current collector film. The continuity of the film is ensured since percolation pathways, i.e. in-plane connectivity, are observed (see inlet of Fig. 2b).

Electrochemical characterization of LSC/YSZ/LSC free-standing symmetrical membranes was carried out on a Probostat cell inside a high temperature furnace. Pt meshes were attached to both sides of the substrate always avoiding direct contact with the membranes to prevent severe damages. Electrochemical impedance spectroscopy (EIS) across the membrane was performed by applying small AC voltages of 50 mV in order to keep the linear regime at the measurement temperature range, in the frequency range from 30 MHz to 0.1 Hz (Novocontrol Alpha-A frequency analyzer with ZG4 test interface). Measurements were performed in temperatures between 150 °C and 700 °C, in order to properly separate the contribution of each component of the cell from the total resistance. Synthetic air was used as oxidizing atmosphere on both sides of the membrane. The Adler-Lane-Steele (ALS) model was applied for fitting the arcs of the porous mixed ionic-electronic conductor LSC [53].

3. Results and discussion

3.1. Microstructural and electrical characterization of porous LSC thin films deposited by PLD

Fig. 3 shows top view and cross section SEM images of as-deposited (a, b) and post-annealed at 700 °C (c, d) LSC porous layers (350 nm-thick) deposited over dense YSZ films. The typical columnar growth of PLD-deposited complex oxides [54] is observed for both the YSZ and LSC layers. However, while YSZ presents strongly ordered and well-defined compact grains, LSC shows disordered columnar clusters with open porosity all along the whole thickness of the films. The origin of these differentiated microstructures corresponds to the set of PLD deposition conditions selected for each material, mainly temperature and pressure. According to Infortuna et al. [54], a high background pressure promotes the mobility of species allowing the formation of single clusters on the film, while the substrate temperature is the responsible of re-crystallization and grain growth during the deposition. Thus, low-temperature and high-pressure depositions, like the ones employed for LSC, usually provide disordered films formed by separated clusters with a high percentage of amorphous phase and porosity. Meanwhile, high-temperature and low-pressure conditions, as employed for YSZ, yield to ordered dense layers. The comparison of the Fig. 3a–d shows the evolution of the microstructure with a thermal treatment up to maximum expected working temperatures ($T = 700\ ^{\circ}C$). While the microstructure of the YSZ layer remains essentially the same, showing a great stability against temperature (see references [6,55] for a more detailed study of the authors on YSZ films), the microstructure of the LSC layers evolves towards an inhomogeneous porosity. Indeed, cracks are apparently observed in the top view image of the layer (Fig. 3c). These cracks are only affecting the upper part of the layer (see Fig. 3d), that is, not affecting the quality of the attachment between the film and the substrate. Indeed, an excellent adhesion between YSZ and LSC is observed by SEM, i.e. no loss of percolation is expected (not measured) after crystallization. This microstructural evolution is likely associated to the combined effect of the crystallization of the film from its initial amorphous nature and the partial sintering and densification of the original clusters into bundles. No cracking or delamination was observed on the fabricated films. By simple image processing of the SEM images, the in-plane porosity was found to be of *ca.* 30% ensuring good percolation, large Triple-Phase-Boundary (TPB) lengths and reasonable diffusion of gas species. Presumably, the observed porosity helps to balance the big difference in thermal expansion coefficient (TEC) reported for both materials, avoiding Sr segregation [37,38,44] and limiting the presence of significant stresses in the final multi-layer.

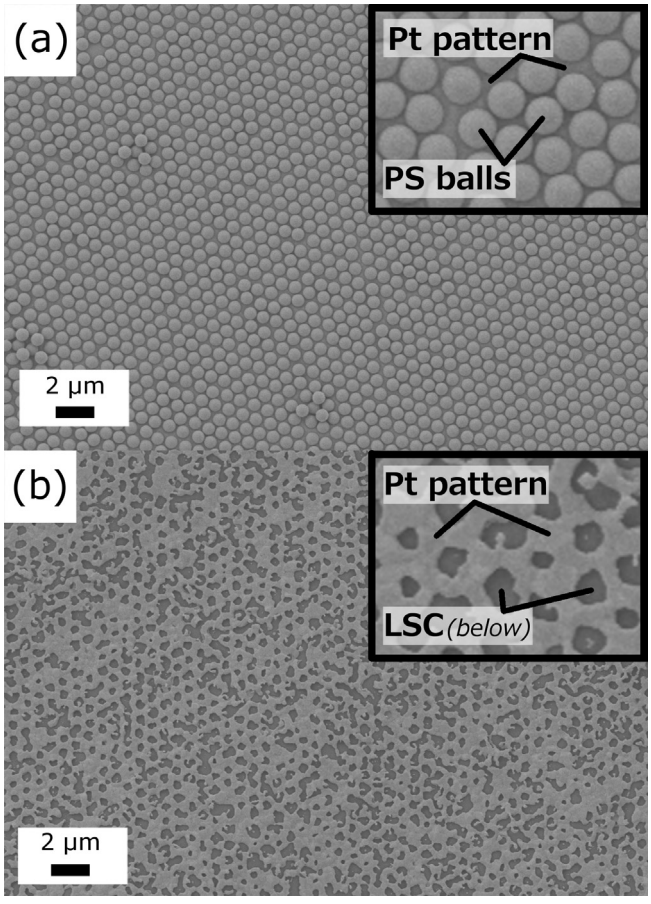

Fig. 2. SEM top view images of a Pt current collector fabricated by nanosphere lithography, as-deposited (a) and post-measurement (b).

Fig. 4 shows the evolution with temperature of the XRD patterns of the LSC/YSZ bi-layer deposited on $Si_3N_4/SiO_2/Si$ substrates from room temperature to 700 °C. The pattern acquired at room temperature corresponds to the as-deposited sample. A single phase is clearly shown by the only presence of diffraction peaks corresponding to a pure cubic *Fm-3m* structure (JCPDS-ICDD #30-1468). A previous work by the authors [6] showed that so deposited YSZ layers present less than 5% vol. of amorphous phase and pure cubic phase (no significant tetragonal contribution). No diffraction peaks are observed for the as-deposited LSC indicating an amorphous nature of the layer prior to annealing. As previously mentioned, this is mainly due to the low substrate temperature employed during the PLD process. The evolution of the XRD patterns with temperature shows a crystallization of the LSC layer between 500 and 550 °C by the appearance of new diffraction peaks corresponding to the cubic *Pm-3m* structure (JCPDS-ICDD #48-0121). The LSC crystallization at such low temperatures is very convenient for reaching the main goal of avoiding high temperature steps in the fabrication process. It is also important to notice that no reactivity between LSC and YSZ was observed up to 700 °C, showing the applicability of LSC on a great range of temperatures covering the typical intermediate temperature range ascribed to the μSOFC.

Fig. 5 shows the evolution of the in-plane conductivity with the temperature on a 350 nm thick LSC film, measured by using the Van

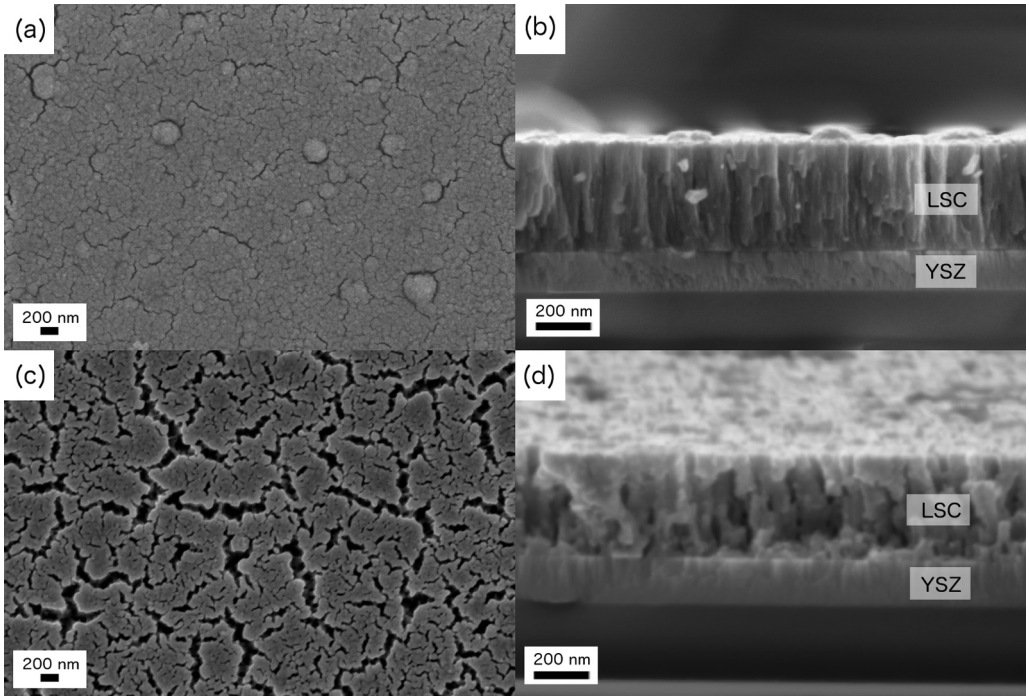

Fig. 3. Top view and cross-section SEM images of as-deposited (a, b) and post-annealing (c, d) 350 nm-thick porous LSC layers over previously deposited dense YSZ.

der Pauw method. Starting from as-deposited samples, an improvement of more than one order of magnitude is observed at $T = 500–525$ °C. Non hysteresis was observed for the subsequent cooling and heating curves, suggesting the irreversibility of the phenomenon. Therefore, and in concordance with the XRD study (Fig. 4), the abrupt change can be associated to the crystallization of the LSC layer and the corresponding increase of electronic conductivity [42]. A maximum value of *ca.* 300 S cm^{-1} on in-plane conductivity is observed after crystallization. This is well over the target values typically required for SOFC electrodes (20 S cm^{-1}), even more assuming the sub-μm size of the fabricated cathode. No degradation or drastic losses in conductivity were observed neither with temperature nor time up to 700 °C and for more than 60 h.

3.2. Microstructural and electrochemical characterization of LSC cathodes implemented in large-area μSOFCs

Fig. 6 shows top view and cross section images (optical and SEM, respectively) of the self-supported large area membranes used for this work, after deposition of YSZ and LSC. The area of the measured membranes is 2.8 mm^2 for a total active area of 2 mm^2, which represents an enhancement of *ca.* 20× over previously reported basic free-standing membrane configurations [3]. The mechanical stability of the membranes is ensured by the grid of silicon slabs (5 μm in thickness). The buckling patterns observed in the free-

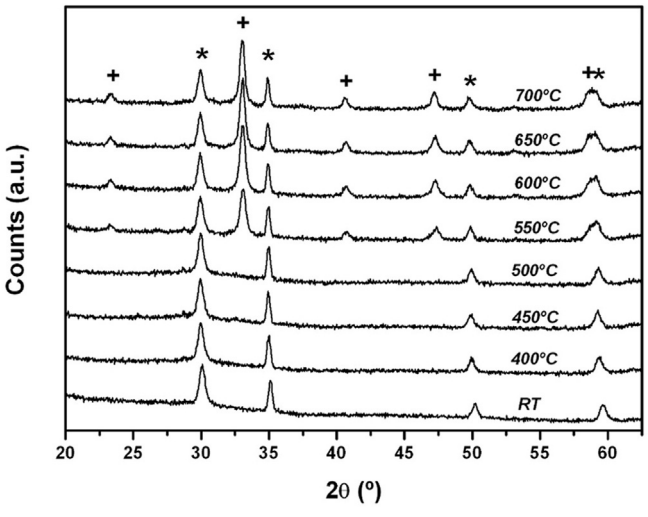

Fig. 4. X-ray diffraction patterns of a porous LSC film deposited over dense YSZ on a $Si_3N_4/SiO_2/Si$ substrate, measured at different temperatures. The stars correspond to YSZ diffraction peaks, while the crosses point out the main peaks of a crystalline LSC pattern, appeared between $T = 500$ °C and $T = 550$ °C.

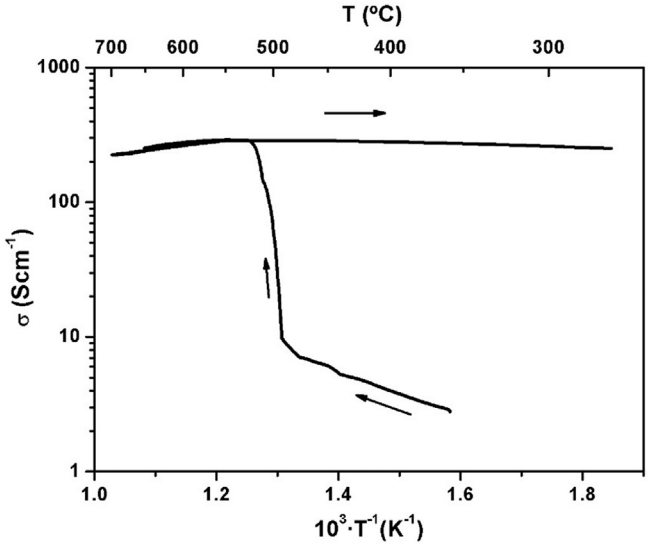

Fig. 5. Evolution of the in-plane conductivity of a porous 350 nm thick LSC cathode deposited over dense YSZ on a $Si_3N_4/SiO2/Si$ substrate, measured by the van der Pauw method.

standing part of the membranes (see Fig. 6a) correspond to a compressive strain mainly associated to the YSZ layer (see references [6,55] for further details on the origin and thermo-mechanical response of the so-strained membranes). The LSC double deposition did not affect the buckling pattern suggesting a minimal contribution from the electrode layer to the total strain (as expected being LSC a porous layer able to easily release stress). The functional tri-layer (LSC/YSZ/LSC) presents a total thickness of *ca.* 1.2 μm with 500 nm of dense YSZ electrolyte and 350 nm of porous LSC at both sides (Fig. 6b).

The LSC/YSZ/LSC membranes were characterized by EIS in order to evaluate their electrochemical performance in the final μSOFC configuration. Fig. 7 depicts two Nyquist plots corresponding to impedance spectra obtained at different temperatures. Below 350 °C, two arcs are clearly observed. A small arc appears at high frequencies due to the resistance associated to the ionic conduction through the bulk electrolyte ($T = 300$ °C spectrum on Fig. 7) while a big arc present at lower frequencies is presumably associated to poor performance at the electrodes. No grain boundary contribution to the resistance was observed for the electrolyte due to the typical columnar growth of PLD-deposited YSZ (see reference [6] for further details).

At higher temperatures, the arc corresponding to the electrolyte becomes a pure serial resistance while the low-frequency arc associated to the symmetrical electrodes shows a great reduction in resistance ($T = 600$ °C spectrum on Fig. 7). The continuous line represents the fitted ALS continuum model [53] useful for describing porous mixed ionic-electronic conductors like LSC, i.e.

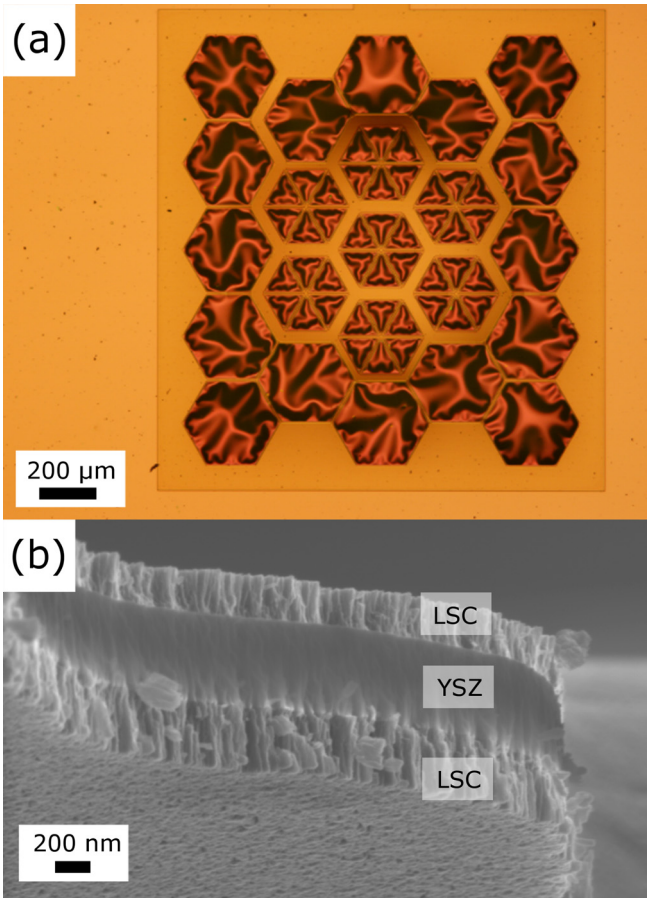

Fig. 6. (a) Top view optical image of a large area YSZ free-standing membrane supported on doped silicon slabs grid. (b) SEM cross sectional view of a flying free-standing LSC/YSZ/LSC tri-layer.

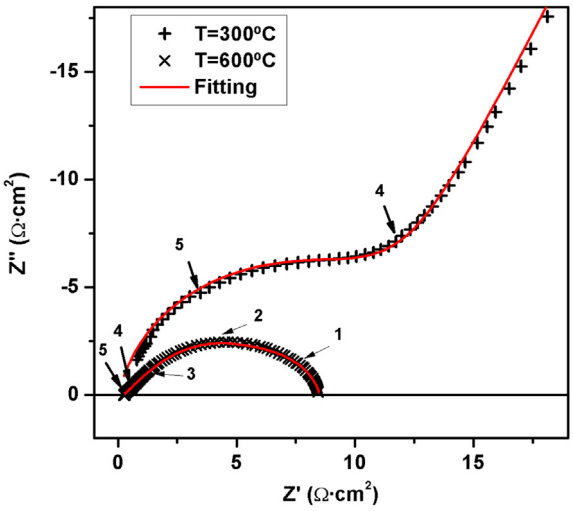

Fig. 7. Impedance spectra of a symmetrical LSC/YSZ/LSC free-standing membrane, measured at $T = 600$ °C and $T = 300$ °C. Solid red lines represent the fitting for the two different spectra. The numbers refer to the frequency decades covered by the EIS analysis. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

the case under study. The excellent agreement between model and experimental data suggests that the non-charge transfer phenomena (solid-state oxygen diffusion and O_2 surface exchange) and the gas-phase diffusion dominate the electrochemical behaviour of the system.

It is important to notice here that the Si diffusion from the substrate is not expected to significantly affect the electrochemical behaviour of the YSZ layer. This is due to the accumulation of silicon in the grain boundaries that present negligible contribution to the total resistance as previously mentioned. SIMS analysis performed after annealing at 800 °C (not presented here) shows that silicon from the substrate does not reach the electrode side through the dense electrolyte. Any asymmetry between the top and bottom electrode is observed by EIS suggesting that possible silicon diffusion from the substrate after RIE is neither significant. All these facts indicate that there is not significant effect of Si diffusion neither in the YSZ nor LSC films electrochemical behaviour. However, future long-term degradation studies have to consider the relevance of this effect with time.

Fig. 8 shows Arrhenius plots of the area-specific-resistance of the electrolyte (ASR_{YSZ}) and the electrolyte–cathode interface (ASR_{LSC}) as a function of the temperature, compared to previously reported values for both materials as well as state-of-the-art Pt electrodes. ASR values were obtained from the equivalent circuit fitting of the set of impedance spectra. Only the active area of the membrane was used for the calculations. The ASR dependence on temperature follows an Arrhenius-type law for both the YSZ and the LSC, with activation energies of $E_a = 1.05(1)$ eV and $E_a = 1.54(4)$ eV, respectively. These values are in concordance with previously reported values for the corresponding bulk materials (see references [31,54,56–58] for YSZ and [21,22,24,42] for LSC).

The YSZ electrolyte presents similar ASR_{YSZ} values than those previously reported for bulk [57] and YSZ free-standing membranes measured in cross-plane [12]. Thus, fabrication of large-area YSZ membranes with similar performances than those already reported was satisfactorily proven. Although film stress has a marked influence on ionic-conduction properties by affecting the charge carrier mobility [59–64], any relevant contribution of the strain on the *cross-plane* conductivity was observed neither in this work nor in previous studies on free-standing YSZ membranes [6]. This is

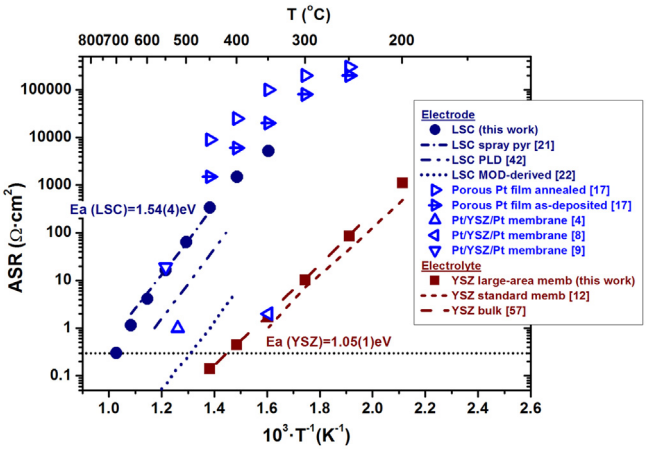

Fig. 8. Evolution of the ASR of both LSC electrode and YSZ electrolyte with temperature, measured on symmetrical LSC/YSZ/LSC free-standing membranes. Reference values from previously published works [4,8,9,12,17,21,22,42,57] are also plotted for comparison. Black dot line marks the 0.3 Ω cm^2 target value for the cathode/electrolyte bi-layer.

probably due to (i) a great reduction of the film stress after buckling deformation and, (ii) a defect clustering and vacancy association taking place close to the grain boundaries, which in cross-plane measurements is much less significant in our columnar-type microstructure. In terms of μSOFC applications, the electrolyte layer should not contribute more than 0.15 Ω cm^2 to the total fuel cell resistance [11]. In the present case, this target was attained at temperatures as low as 450 °C, covering the typical μSOFC temperature range (500–700 °C).

LSC resistivity values were similar or slightly higher than other previously reported thin films of LSC (some of them also plotted on the figure for direct comparison [21,22,42]). This small discrepancy can be attributed to the well-known dependency of the oxygen surface exchange properties and electrolyte-electrode polarization resistances on the fabrication routes. Up to the authors' best knowledge, this is the first report on half-cell measurements of a thin film LSC/YSZ/LSC system and, therefore, it is not possible to directly compare the obtained ASR with any similar configuration previously reported.

As earlier mentioned, Fig. 8 also includes ASR values for two different porous Pt/YSZ interfaces: (i) based on Pt/YSZ/Pt membranes under real μSOFC operating conditions from three different research groups [4,8,9]; (ii) based on porous Pt films deposited on YSZ single crystal as reported by Ryll et al. [17]. The wide variability of reported values is probably due to the instability of these metallic-based electrodes at μSOFC operating temperatures and does not allow clear comparison with the here presented results on LSC's performance.

An absolute value usually targeted for cathode/electrolyte polarization resistances is ASR = 0.3 Ω cm^2 [11]. In this sense, the here-presented results suggest the need of temperatures higher than 650 °C for having a good performance of the LSC/YSZ interface (dot line in Fig. 8). Although this fact forces to work at higher temperatures than those previously published μSOFC devices based on Pt/YSZ/Pt (350–550 °C, [3,13]), the proven stability of the LSC films at such temperatures makes the system more reliable considering the fast degradation observed for pure metallic based devices. Moreover, working at such high temperatures allows substantially increasing the electrolyte thickness to several hundreds of nm. Thicker electrolytes make the membrane more robust reducing the probability of pinhole formation, i.e. minimizing one of the most frequent reasons of dramatic failure for free-standing electrolyte membranes [12].

4. Conclusions

Highly porous LSC thin films (up to 33% in-plane porosity) were deposited by PLD over dense YSZ films for the fabrication of bi-layer cathode/electrolyte free-standing membranes for micro solid oxide fuel cells applications. An in-plane conductivity of *ca.* 300 S cm^{-1} was measured for the porous LSC films, within the typical range of μSOFC operation temperatures (450–700 °C), well over the values typically required for SOFC cathodes. Any microstructural degradation or loss of in-plane conductivity was observed neither with temperature nor with time up to 700 °C and for more than 60 h. The fabrication process of a novel large-area membrane design is detailed. This membrane is employed for the implementation and evaluation of LSC porous layers as a cathode into a real μSOFC configuration, i.e. symmetrical LSC/YSZ/LSC free-standing membrane cell. The thermo-mechanical stability of the large-area membranes was ensured up to 700 °C. Target values of Area Specific Resistance required for SOFC cathode/electrolyte interface (ASR = 0.30 Ω cm^2) were achieved in the intermediate range of temperatures (T = 700 °C). These results showed the feasibility of using the fabricated LSC as cathode on μSOFC configurations, as a good alternative to the widely used metallic electrodes and anticipating more reliable all-ceramic-based micro solid oxide fuel cells operating in the intermediate range of temperatures.

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